

**Face-Down Chip-on-Wafer Bonding**: System-in-package (SiP) solutions for mobile and wearable devices must be thin and have a small overall footprint, but conventional SiP devices using organic substrates and solder interconnects are reaching their size limits. Also, managing wafer warpage during processing is critical due to mismatched coefficients of thermal expansion among the various system components. At ECTC, a Murata-led team in WOW Alliance of Science Tokyo will propose a Face-Down Chip-on-Wafer (FD COW) process to address these challenges. It makes use of a waffle wafer stack structure that enables bumpless via-last interconnects. Waffle wafers have a patterned grid-like structure on their surface which enables them to be very thin; their reduced volume mitigates warpage. For FD COW bonding to become practical, the adhesive coating used must be enhanced and uniform distribution of that adhesive must be ensured on the trench surfaces of the waffle wafer. It is also essential to optimize chip bondability and to minimize misalignment under high-speed bonding conditions. The researchers will describe an innovative selective adhesive coating method, and evaluate its compatibility with high-speed chip bonding for bumpless FD COW using a single waffle wafer. Through the development of this process, >30,000 chips of several different sizes were bonded at 40 µm spacing, achieving >20X faster bonding speed without any chip-detachment failures. The researchers say the face-down COW process is highly promising for high-speed, high-density heterogeneous bonding applications.

* **The images above** are (top left) an SEM image of the FD COW structure; (top right) the trench area on the waffle wafer demonstrating 40 µm spacing; (bottom row) schematics comparing conventional SiP dimensions with 1- and 2- layer FD COW architectures.

**(Paper 1.2, “*Face-Down Bonding and Heterogeneous Chiplet Integration by Using Bumpless Chip-on-Wafer (COW) with Waffle Wafer Technology*,” Y. Satake et al, Murata/Institute of Science Tokyo/Panasonic Connect Co. Ltd**)